IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TELCORDIA TECHNOLOGIES, INC., Plaintiff/Counterclaim Defendant, v. LUCENT TECHNOLOGIES INC., Defendant/Counterclaim Plaintiff.	)	**REDACTED** **PUBLIC VERSION** Civil Action No. 04-875-GMS
TELCORDIA TECHNOLOGIES, INC., Plaintiff/Counterclaim Defendant, v. CISCO SYSTEMS, INC., Defendant/Counterclaim Plaintiff.	)	Civil Action No. 04-876-GMS

TELCORDIA TECHNOLOGIES, INC.'S MOTION *IN LIMINE* NO. 4:

MOTION TO PRECLUDE TESTIMONY ON ALLEGED INEQUITABLE CONDUCT DURING PROSECUTION OF THE '633 PATENT BASED UPON (1) THE GONZALES ARTICLE OR (2) PRIVATE COMMUNICATIONS WITH FRANCE TELECOM

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177599.1

I. INTRODUCTION

Defendants Lucent Technologies, Inc. ("Lucent") and Cisco Systems, Inc. ("Cisco") should be precluded from presenting testimony or making arguments at trial that Telcordia's '633 patent is unenforceable due to inequitable conduct based on certain contentions that information was withheld from the U.S. Patent and Trademark Office during prosecution of U.S. Patent Re. 36,633 ("the '633 patent").

Specifically, defendants should not be permitted to present the following arguments or testimony supporting those arguments: (1) that there was inequitable conduct based on a supposed mischaracterization of the Gonzales article in the patent specification, where the article was given to and reviewed by the patent examiner; and (2) that there was inequitable conduct relating to private communications to Telcordia from France Telecom. As to the Gonzales article, the PTO had the Gonzales article, no information regarding the article was withheld, and the examiner was free to review the information in the specification, compare it to the article, and reach his own conclusions concerning its relevance.

Similarly, non-disclosure of the France Telecom communications during prosecution of the application that led to U.S. Patent No. 5,260,978 ("the '978 patent"—the parent to the reissued '633 patent) is not inequitable conduct. The private France Telecom communications were not recognized as constituting potential prior art at that time, and as such there was no duty to disclose this type of information. Only after the prosecution of the '978 patent did the Federal Circuit "settle the persistent question [of] whether § 102(f) is a prior art provision for purposes of § 103." *OddzOn Prods., Inc. v. Just Toys, Inc.*, 122 F.3d 1396, 1402 (Fed. Cir. 1997). And since the communications from France Telecom were disclosed during the prosecution of the '633 patent (after the *OddzOn* decision), these communications cannot form the basis of an inequitable conduct claim.

Defendants' arguments are legally incorrect and cannot succeed, and defendants' insistence on pursuing them at trial is a naked attempt to prejudice Telcordia.

II. ARGUMENT

The Federal Circuit has recognized that allegations of inequitable conduct are made in almost every major patent case, irrespective of whether the allegation is supported. In *Burlington Indus., Inc. v. Dayco Corp.*, 849 F.2d 1418, 1422 (Fed. Cir. 1988), for example, the Court stated that "the habit of charging inequitable conduct in almost every major patent case has become an absolute plague." Similarly, in *Ortho Pharmaceutical Corp. v. Smith*, 18 U.S.P.Q.2d 1977, 1991 (E.D. Pa. 1990), *aff'd*, 959 F.2d 936 (Fed. Cir. 1992), the Court noted that inequitable-conduct is a "much-abused" allegation:

> Inequitable conduct is a much-abused and too often last-resort allegation. . . . As in many patent cases, the issue of inequitable conduct deflects the court's attention from the issues of validity and infringement. . . . [A challenger] in complex litigation should not be permitted to sidestep these main issues by nit-picking the patent file in every minute respect with the effect of trying the patentee personally, rather than the patent.

Defendants' only hope in raising the frivolous inequitable conduct defenses addressed in this motion is to deflect attention from the substantive issues of infringement and validity and, more seriously, inflame the jury unfairly against Telcordia merely by mouthing the words "fraud on the Patent Office" or "inequitable conduct." That tactic should not be allowed, and defendants should be precluded from trying to bolster their inequitable conduct positions with facially improper arguments and evidence.

A. The Gonzales Article Was Before The PTO And The Examiner Had The Opportunity To Evaluate Telcordia's Comments About The Article

The Gonzales article (Gonzales et al., "*Jitter Reduction in ATM Networks*," Proceedings ICC '91, 9.4.1-9.4.6) was not only disclosed to the PTO, it was discussed in the patent specification and cited by the patent examiner on the face of both the original '978 patent and the '633 reissue patent. (Ex. A, '633 patent, page 2 and col. 2, line 64 to col. 3, line 38; Ex. B, '978 patent, page 2). Defendants' expert Dr. Jones stated,

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But even assuming, *arguendo*, that the specification's description of Gonzales is inaccurate—an assertion with which Telcordia does not agree—

that does not compel a finding of inequitable conduct because the entire article was before the examiner and he was free to review the article and reach his own conclusions about its disclosures. *See, e.g., Akzo N.V. v. U.S. Int'l Trade Comm'n*, 808 F.2d 1471, 1482 (Fed. Cir. 1986) (no inequitable conduct based on arguments before the PTO regarding two prior art references where "[t]he examiner was free to reach his own conclusion regarding the [claimed invention] based on the art in front of him"); *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573, 1581 (Fed. Cir. 1997) (no inequitable conduct as a result of arguments regarding disclosure in reference where "the examiner himself had located and cited the German '756 patent, and could consult it while evaluating Gambro's comments in response to his office action.").

Since defendants cannot prevail on their inequitable conduct contention with regard to the description of the Gonzales article, they should be prohibited from attempting to introduce evidence or argument in furtherance of that contention in order to avoid prejudice to Telcordia.

B. The France Telecom Communications Were Disclosed To The PTO During The Reissue Proceeding And Were Not Required To Be Disclosed During The Original Prosecution

Defendants also cannot prevail on any inequitable conduct argument based on the supposed failure to disclose to the PTO the private communications from France Telecom to Telcordia's predecessor, Bell Communications Research, Inc. ("Bellcore"). The inventors disclosed these communications during the reissue proceeding, and the law did not require the inventors to disclose private communications during prosecution of the original '978 patent.

In his report, defendants' expert Mr. Jones

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Still, the October 11 memo was disclosed during the reissue proceeding and cited as a reference. (Ex. A, cover page). The remaining documents—the August 26 letter, the October 14 facsimile, and the undated memo (i.e., the communications from France Telecom)—were also disclosed during the reissue and cited on the face of the patent. (Ex. A, cover page).

The France Telecom communications were not cited during the prosecution of the '978 patent, but the law did not require the inventors to disclose such private communications. The France Telecom communications were not publications or public uses of the invention, so they were not prior art under 35 U.S.C. §§ 102(a) or (b). Even if they evidenced a prior invention by France Telecom—which they most assuredly did not—such invention was not prior art under § 102(g) because it was not in the United States. Again, assuming the communications support the defendants' contentions—which they do not—the communications at best bear only upon whether the invention was allegedly derived from another source, namely France Telecom, in violation of § 102(f). Moreover, the critical communication—the early facsimile on August 21—does not describe the entire claimed invention within its four corners, so it cannot anticipate the asserted claims. Instead, as Mr. Jones admitted in his deposition,

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(Ex. C). In other words, the defendants are combining the France Telecom facsimile with several other references in an obviousness argument under § 103.

But when the original patent was being prosecuted between 1992 and 1993, § 102(f) information was not generally considered prior art that could be combined with other materials to render an invention

obvious. *OddzOn Prods., Inc. v. Just Toys, Inc.*, 122 F.3d 1396, 1402 (Fed. Cir. 1997). Only after the 1997 *OddzOn* decision, in which the Federal Circuit "settle[d] the persistent question whether § 102(f) is a prior art provision for purposes of § 103," would an inventor understand that § 102(f) information lacking all the elements of the claimed invention, like the France Telecom communications, might still be combined with other prior art to render his invention obvious, and that such information therefore should be disclosed to the PTO. *Id.* Since the '978 patent issued in 1993, long before that issue was settled by the Federal Circuit, the non-disclosure of the private France Telecom communications cannot constitute inequitable conduct.

III. CONCLUSION

For the reasons stated above, Telcordia respectfully requests that the Court prohibit defendants from presenting testimony or making arguments that the '633 patent is unenforceable due to inequitable conduct based on (1) the supposed inaccurate description in the patent specification of the Gonzales article or (2) the failure to disclose the France Telecom communications during the prosecution of the '978 patent.

ASHBY & GEDDES

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EXHIBIT A

US00RE36633E

United States Patent [19]

Fleischer et al.

[11] E Patent Number: Re. 36,633

[45] Reissued Date of Patent: Mar. 28, 2000

[54] SYNCHRONOUS RESIDUAL TIME STAMP FOR TIMING RECOVERY IN A BROADBAND NETWORK

[75] Inventors: Paul E. Fleischer, Little Silver; Chi-Leung Lau, Marlboro, both of N.J.

[73] Assignee: Telcordia Technologies, Inc., Morristown, N.J.

[21] Appl. No.: 08/555,196

[22] Filed: Nov. 8, 1995

Related U.S. Patent Documents

Reissue of:

[64] Patent No.: 5,260,978
Issued: Nov. 9, 1993
Appl. No.: 07/969,592
Filed: Oct. 30, 1992

[51] Int. Cl.^{7} H04L 7/00

[52] U.S. Cl. 375/354; 375/362; 375/364; 370/509; 370/394; 370/516

[58] Field of Search 375/354, 355, 375/362, 365, 366, 371, 364; 370/503, 509, 510, 511, 512, 516, 394, 517, 519

[56] References Cited

U.S. PATENT DOCUMENTS

4,489,421 12/1984 Burger .
4,530,091 7/1985 Crockett .
4,759,014 7/1988 Decker et al. .
4,961,188 10/1990 Lau .
5,115,431 5/1992 Williams et al. .
5,255,291 10/1993 Holden et al. .

FOREIGN PATENT DOCUMENTS

3-114333 5/1991 Japan .

OTHER PUBLICATIONS

CCITT Study Group XVIII/8—Contribution D. 1123 entitled "Proposed method to provide the clock recovery function for circuit emulation", (Dec. 1990).

Letter from P. Adam of CNET dated Aug. 26, 1991 concerning discussion on TS/SFET.

Memorandum from R. Lau and B. Kittams of Bellcore dated Oct. 11, 1991 re A Compromise of SFET and TS.

Memorandum from T. Houdoin to B. Kittams & R. Lau dated Oct. 14, 1991 re Compromise SFET/TS.

CNET Memorandum from T. Houdoin to R. Lau and B. Kittams re Compromise SFET/TS (undated).

Y. Matsuura, S. Kozuka, K. Yuki, "Jitter Characteristics of Pulse Stuffing Synchronization," pp. 259–264, Jun. 1968.

D.L. Duttweiler, "Waiting Time Jitter," *Bell System Technical Journal*, vol. 51, No. 1, pp. 165–209, Jan. 1972.

CCITT Recommendations G. 707, G. 708, G. 709 (1988).

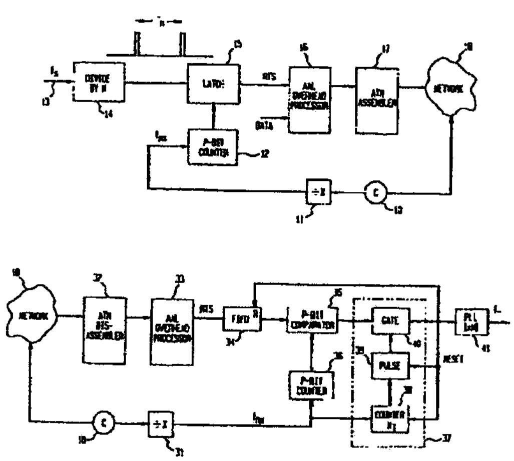
(List continued on next page.)

Primary Examiner—Don N. Vo
Attorney, Agent, or Firm—Joseph Giordano

[57] ABSTRACT

A Residual Time Stamp (RTS) technique provides a method and apparatus for recovering the timing signal of a constant bit rate input service signal at the destination node of a synchronous ATM telecommunication network. At the source node, a free-running P-bit counter counts cycles in a common network clock. At the end of every RTS period formed by N service clock cycles, the current count of the P-bit counter, defined as the RTS, is transmitted in the ATM adaptation layer. Since the absolute number of network clock cycles likely to fall within an RTS period will fall within a range determined by N, the frequencies of the network and service clocks, and the tolerance of the service clock, P is chosen so that the 2_p possible counts, rather than representing the absolute number of network clock cycles an RTS period, provide sufficient information for unambiguously representing the number of network clock cycles within that predetermined range. At the destination node, a pulse signal is derived in which the periods are determined by the number of network clock cycles represented by the received RTSs. This pulse signal is then multiplied in frequency by N to recover the source node service clock.

33 Claims, 3 Drawing Sheets



OTHER PUBLICATIONS

CCITT Recommendations G. 823, G. 824 (1988).
CCITT Recommendations D.294, "Timing for CBO Services," Jun. 1989.
R.C. Lau, "Synchronous Frequency Encoding Technique for B-ISDN Circuit Emulation," SPIE vol. 1179 Fiber Networking and Telecommunications, pp. 160-171, Sep. 1989.
H.M. Ahmed, "Adaptive Terminal Synchronization in Packet Data Networks," Globecom, pp. 20.6.1-20.6.5, 1989.
CCITT SG XVIII Contribution, D.1020, "Timing Recovery for CBR Circuit Emulation." Dec. 1990.
CCITT Study Group XVIII—Contribution D. 1451 entitled "Performance Comparison of Timing Recovery Methods for CBR Services," Jun. 1991.
Submission to T1S1 entitled "Broadband Aspects of ISDN," T1S1.5/91-382, Nov. 4, 1991.
Summary Minutes of T1 Services, Architecture, and Signaling Technical Subcommittee (T1S1) Session, Nov. 8, 1991.
CCITT Study Group XVIII entitled "Synchronous Residue-Time Stamp: A Combination of SFET/TS", Dec. 1991.
CCITT Study Group XVIII entitled "Report of the meeting of SWP XVIII/8-3 (Services, IVS and AAL types 1 and 2)", Dec. 1991.
CCITT Study Group XVIII entitled "Revised text of I.363 Section 2 (AAL type 1)", Dec. 1991.
CCITT Recommendation I.363 entitled "B-ISDN ATM Adaptation Layer (AAL) Specification," (1991).
Appendix 5 (to Annex 7) for COM XVIII-R 70-E entitled "Descriptions of the SFET Method" (Jul. 1991).
Appendix 6 (to Annex 7) for COM XVIII-R 70-E entitled "Descriptions of the TS Method" (Jul. 1991).
R.C. Lau and P.E. Fleischer, "Synchronous Techniques for Timing Recovery in BISDN," *IEEE Globecom*, pp. 814-820, Dec. 1992.
R.C. Lau and P.E. Fleischer, "Synchronous Techniques for Timing Recovery in BISDN," Communications Switching of the IEEE Communications Society, IEEE Transactions on Communications, Apr. 1995.
Kozuka, "Phase Controlled Oscillator for Pulse Stuffing Synchronization System," Review of the Electrical Communications Laboratory, vol. 17, Nos. 5-6, May-Jun. 1969.
R.P. Singh et al., "Jitter and Clock Recovery for Periodic Traffic in Broadband Packet Networks," Bell Communications Research, Inc., presented at IEEE Globecom, Florida, Dec. 1988.
J. Gonzales et al., Proceedings ICC '91, "Jitter Reduction in ATM Networks," 1991, pp. 274-279.
R.P. Singh et al., "Adaptive Clock Synchronization Schemes for Real-Time Traffic in Broadband Packet Networks," Presented-8th European Conference on Electrotechnics, Stockholm, Sweden, Jun. 1988.
American National Standard, ANSI T1.105-1988, "Digital Hierarchy Optical Interface Rates and Formats Specification," Sep. 1988.
"Jitter Reduction in ATM Networks," Julio Gonzales and Jean-Paul Le Meur Proceedings ICC '91, 9.4.1-9.4.6.

FIG. 1

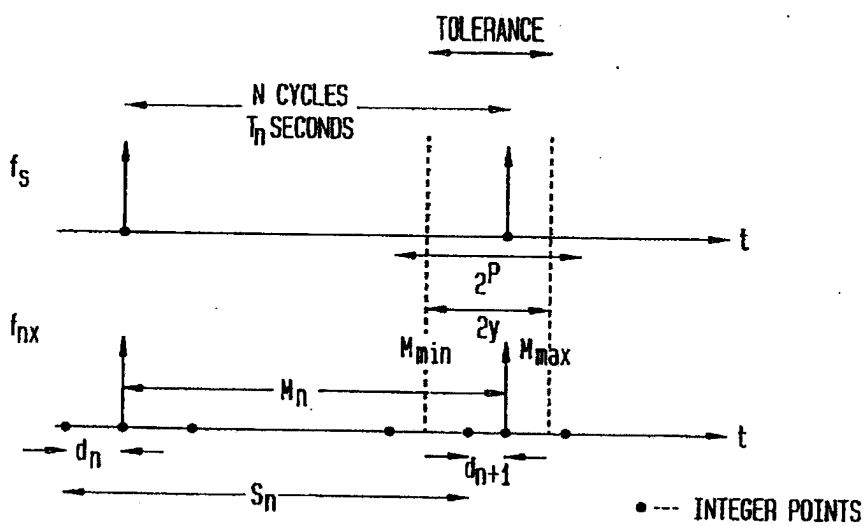
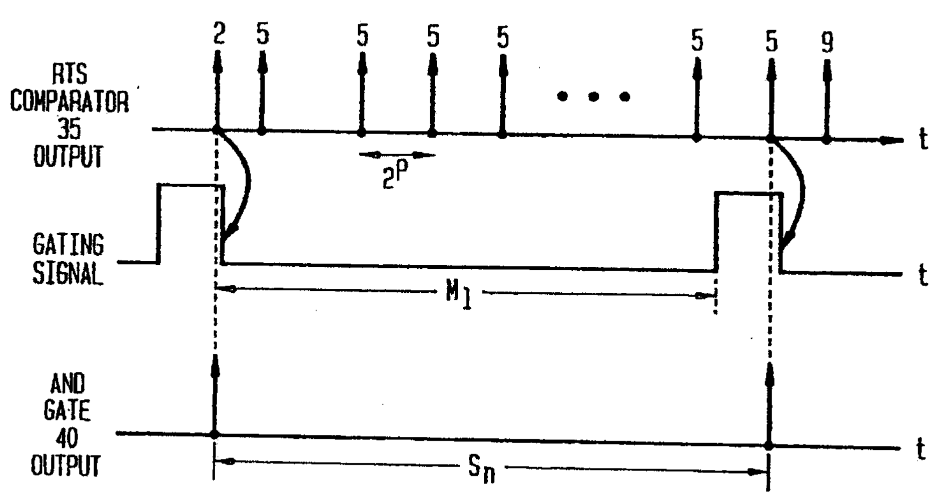

TOLERANCE
N CYCLES
Tn SECONDS
fs
t
2P
fnx
2y
Mmin
Mmax
Mn
t
dn
dn+1
Sn
• --- INTEGER POINTS

FIG. 4


2
5
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RTS COMPARATOR 35 OUTPUT
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2P
GATING SIGNAL
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M1
AND GATE 40 OUTPUT
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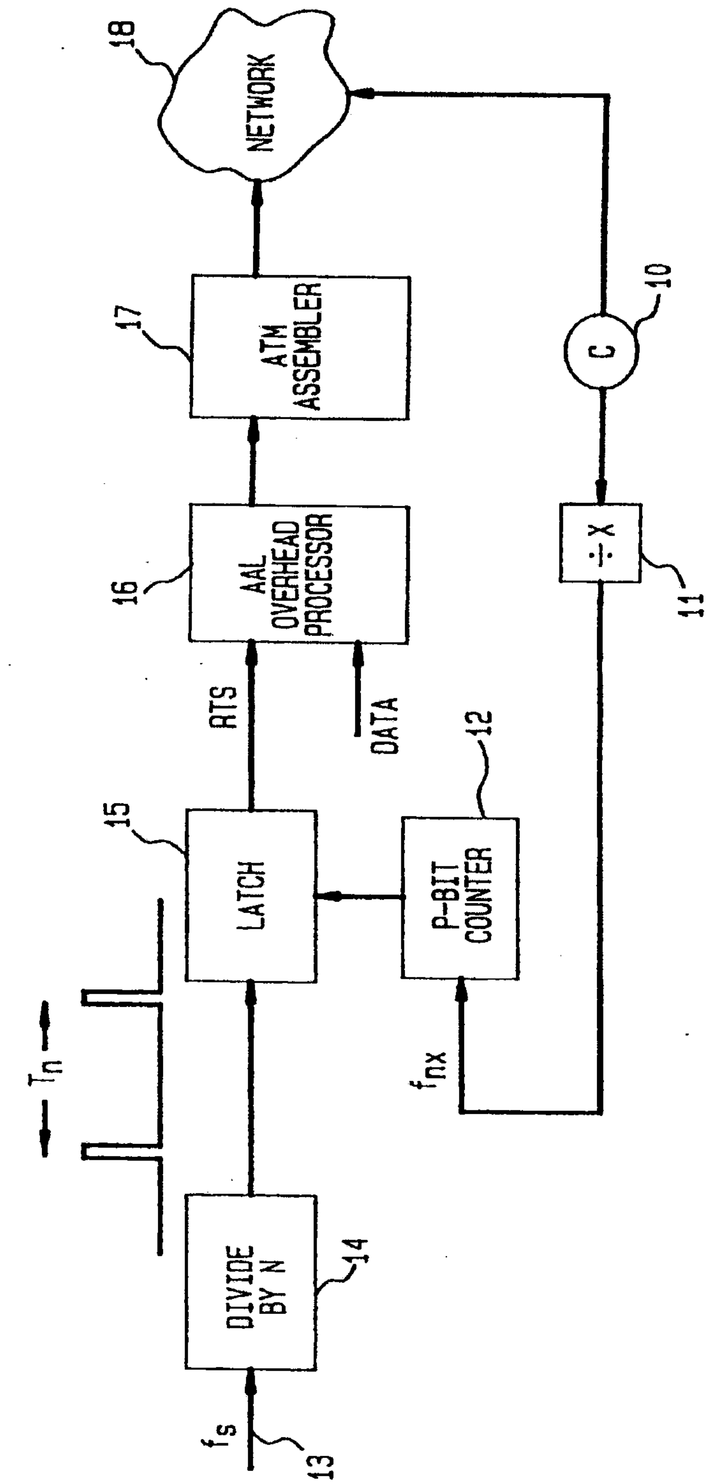
FIG. 2


NETWORK
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ATM ASSEMBLER
17
AAL OVERHEAD PROCESSOR
16
RTS
DATA
LATCH
15
P-BIT COUNTER
12
DIVIDE BY N
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f_s
13
T_n
f_{nx}
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÷ X
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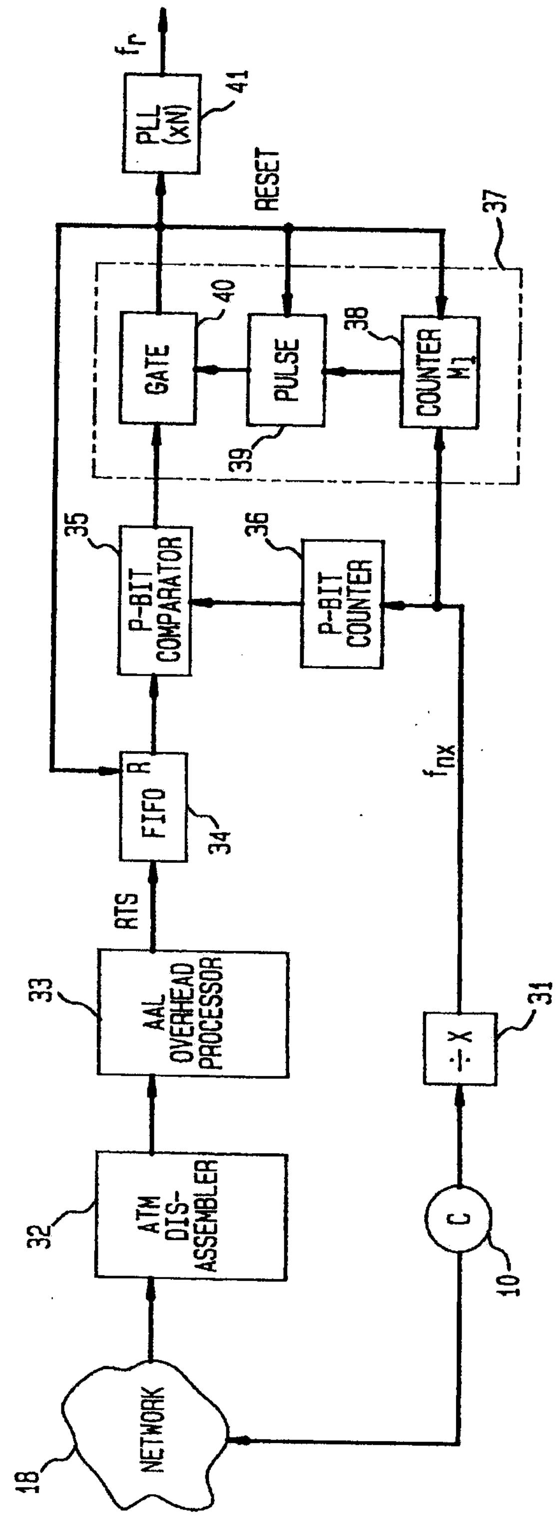
NETWORK
18
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FIG. 3

SYNCHRONOUS RESIDUAL TIME STAMP FOR TIMING RECOVERY IN A BROADBAND NETWORK

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

This application is the parent application of reissue application 09/292,668 filed Apr. 16, 1999.

BACKGROUND OF THE INVENTION

This invention relates to timing recovery of a source node service clock frequency at a destination node in a broadband asynchronous transfer mode (ATM) network where the source and destination nodes receive reference timing signals derived from a single master clock.

Asynchronous Transfer Mode (ATM) is a packet oriented technology for the realization of a Broadband Integrated Services Network (BISDN). By using ATM, network resources can be shared among multiple users. Moreover, various services including voice, video and data can be multiplexed, switched, and transported together under a universal format. Full integration will likely result in simpler and more efficient network and service administration and management. However, while conventional circuit-switching is optimized for real-time, continuous traffic, ATM is more suitable for the transport of bursty traffic such as data. Accommodation of constant bit rate (CBR) services is, however, an important feature of ATM, both for universal integration and for compatibility between existing and future networks. In the transport of a CBR signal through a broadband ATM network, the CBR signal is first segmented into 47-octet units and then mapped, along with an octet of ATM Type I Adaptation Layer (AAL) overhead, into the 48-octet payload of the cell. The cells are then statistically multiplexed into the network and routed through the network via ATM switches.

It is essential to the proper delivery of such CBR service traffic in a broadband network that the clock controlling the destination node buffer be operating at a frequency precisely matched to that of the service signal input at the source node in order to avoid loss of information due to buffer over- or under-flow. However, unlike the circuit-switched transport of service data wherein the clock frequency at the destination node may be traced directly back to that of the source node by the regular, periodic arrival of the CBR traffic, transport in an ATM network inherently results in cell jitter, i.e. the random delay and aperiodic arrival of cells at a destination node, which essentially destroys the value of cell arrival instances as a means for directly recovering the original service signal input frequency.

Such cell jitter, generally the result of the multiplexing of transport cells in the broadband network and the cell queuing delays incurred at the ATM switches in the network, is substantially unpredictable. Thus, little is known about the cell arrival time beyond the fact that the average cell delay is a constant, assuming that the ATM network provides sufficient bandwidth to ensure against loss of cells within the network. As a means for closely approximating the service signal frequency at the destination node, some consideration had previously been given to utilizing a direct extension of circuit-switched timing recovery practices which rely entirely upon a buffer fill signal as the basis for recovery of the source timing. However, due to the lack of knowledge of statistics of the cell jitter, this approach would have required a phase-locked loop with very low cut-off frequency (in the order of a few Hz) and would thus have resulted in excessive converging time and degradation of jitter and wander performance.

A number of schemes have been proposed to improve upon such a conventional manner of recovering service timing in the presence of cell jitter, yet none has achieved this end economically and without extensive control systems of notable complexity. Singh et al., for example, in "Adaptive Clock Synchronization Schemes For Real-Time Traffic In Broadband Packet Networks," 8th European Conference on Electrotechnics, Stockholm, Sweden, June 1988, and "Jitter And Clock Recovery For Periodic Traffic In Broadband Packet Networks," IEEE Globecom '88, Florida, December 1988, have proposed algorithms which attempt to more closely estimate cell jitter statistics and derive timing recovery from those indications. These adaptive approaches, suggested to be applicable to both synchronous and non-synchronous networks, rely upon the interaction of increasingly complex algorithms which would require the noted extensive controls for implementation.

These prior art schemes described above can be classified as non-synchronous techniques, which are based on the simple fact that the expected value of the network cell jitter is zero and thus rely on phase filtering. Synchronous techniques, on the other hand, utilize the fact that common timing is available at both the transmitter and the receiver. In a synchronous broadband ATM network, such as the Synchronous Optical Network (SONET) prescribed by American National Standard, ANSI T1.105-1988, "Digital Hierarchy Optical Interface Rates and Formats Specification," Mar. 10, 1988, the network source and destination node control clocks are synchronized to the same timing reference. As a result, there is no necessity for relying upon any extraneous phenomenon such as instants of cell arrival to provide a datum base for determining the relative frequencies of those control clocks. The effect of cell jitter caused by multiplexing and switching delays in the network is therefore of little consequence in any procedure for circuit transporting CBR service, which is based, as is the present invention, on an actual synchrony of node timing. Thus being devoid of concern for cell jitter, this process is free to simply determine the difference in frequency between the CBR service signal input at the source node and the source/destination node timing clock(s).

U.S. Pat. No. 4,961,188 issued on Oct. 2, 1990 to Chi-Leung Lau, co-inventor herein, discloses a synchronous frequency encoding technique (SFET) for clock timing in a broadband network. The SFET takes advantage of the common timing reference at both the source and the receiver. At the source, the asynchronous service clock is compared to the network reference clock. The discrepancy between properly chosen submultiples of the two clocks is measured in units of a preassigned number of slip cycles of network clock. This clock slip information is conveyed via a Frequency Encoded Number (FEN) which is carried in the ATM Adaptation Layer (AAL) overhead. At the receiver, the common network clock and the FEN are used to reconstruct the service clock. This timing recovery process does not rely on any statistics of the cell jitter except that it has a known, bounded amplitude. Therefore, the recovered clock has jitter performance comparable to that of the circuit-switched network.

An alternative proposed approach is known as Time Stamp (TS). In the Time Stamp approach (see, for example, Gonzales et al, "Jitter Reduction in ATM Networks", Proceedings ICC'91, 9.4.1–9.4.6), the network clock is used to

drive a multi-bit counter (16-bits in the proposal), which is sampled every fixed number of generated cells (e.g., 16). Thus, a fixed number, N, of service clocks cycles is used as the measuring yardstick. The sampled value of the 16-bit counter is the TS that inherently conveys the frequency difference information. Because of the size of the TS (2 octets), it has been proposed that the TS be transmitted via the Convergence Sublayer (CS) overhead. Thus the TS is a 16-bit binary number occurring once every N service clock cycles. Differences in successive TSs represent the quantized values of M, where M is the number of network clock cycles during the fixed TS period. At the receiver, the TS period is reconstructed from the received TSs and the network clock. A free-running 16-bit counter is clocked by the network clock and the output of the counter is compared to the received TSs which are stored in a TS FIFO. A pulse is generated whenever there is a match between the TS and the 16-bit counter. The service clock is recovered by supplying the resultant pulse stream as the reference signal to a multiply-by-N phase locked loop (PLL).

A comparison of the SFET approach and the TS approach reveals advantages and disadvantages for each. In the SFET approach there is a relatively stringent requirement on the derived network clock since it must be slightly larger than the service clock. Advantageously, however, a convergence sublayer is not required to transmit the FEN and only small overhead bandwidth is required to transmit the necessary information. On the other hand, the TS approach is more flexible in that it does not require stringent relationships between the service clock and the network derived clock and can therefore support a range of service bit rates. Disadvantageously, however, a rigid convergence sublayer structure is required to transmit the TS, which adds complexity and makes inefficient use of the overhead bandwidth.

An object of the present invention is to achieve synchronous timing recovery with an approach that has the advantages of both the SFET and TS approaches, specifically, the efficiency of SFET and the flexibility of TS.

SUMMARY OF THE INVENTION

As described hereinabove, the TS approach requires a large number of bits (16-bits in the example), to represent the number of network clock cycles within a time interval defined by a fixed number (N) of service clock cycles. In accordance with the present invention, the number of bits required to represent the number of network clock cycles within that time interval is substantially reduced. This is possible through the realization that the actual number of network clock cycles, M (where M is not necessarily an integer), deviates from a nominal known number of cycles by a calculable deviation that is a function of N, the frequencies of the network and service clocks, and the tolerance of the service clock. Specifically, therefore, rather than transmitting a digital representation of the quantized actual number of network clock cycles within the interval, only a representation of that number as it exists within a defined window surrounding an expected, or nominal, number of network clock pulses is transmitted from a source node to a destination node in an ATM network. This representation will be referred to hereinafter as the Residual Time Stamp (RTS). By selecting the number of bits, P, so that all 2_P possible different bit patterns uniquely and unambiguously represent the range of possible numbers of network clock cycles within the fixed interval that is defined by N service clock cycles, the destination node can recover the service clock from the common network clock and the received RTS.

At the source node, a free-running P-bit counter counts clock cycles in a clock signal derived from the network clock. The service clock, which is derived from the incoming data signal to be transmitted over the ATM network, is divided by the factor of N to produce a pulse signal having a period (the RTS period) which defines the time interval for measuring the number (modulo 2^P) of derived network clock pulses. At the end of each RTS period, the current count of the free-running P-bit counter is sampled. That sampled value is the RTS, which is transmitted via the adaptation layer. Since the service clock from which the RTS period is defined and the derived network clock are neither synchronized nor integrally related in frequency, the actual number of derived network clock cycles in a RTS period is unlikely to be an integer. Thus, when sampled at the end of each RTS period, the increment in the count of the P-bit counter is a quantized version of the count (modulo 2^P) of pulses in the RTS interval as modified by any accumulated fractional counts from a previous interval.

At the destination node, after the AAL is processed, the successive RTSs are converted into a pulse signal which has periods between pulses defined by the fixed integral numbers of derived network clock pulses that correspond to the conveyed RTS periods. Specifically, a free-running P-bit counter is driven by the derived network clock. A comparator compares this count with a stored received RTS and produces a pulse output upon a match. Since the count of the P-bit counter matches the stored RTS every 2_P derived network clock cycles, comparator output pulses that do not actually represent the end of the RTS period are inhibited by gating circuitry. This gating circuitry includes a second counter that counts the derived network clock cycles occurring since the end of the previous RTS period. When this second counter reaches a count equal to the minimum possible number of derived network clock pulses within an RTS period, the next comparator pulse output produced upon a match between the RTS and the count of the P-bit counter, is gated-through to the output and resets the second counter. The resultant gated through output pulse stream drives a multiply-by-N phase locked loop to recover the service clock.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 are timing diagrams showing the RTS concept of the present invention;

FIG. 2 is a block diagram showing apparatus, in accordance with the present invention, for generating the RTS at the source node of an ATM network;

FIG. 3 is a block diagram showing apparatus, in accordance with the present invention, for reconstructing the service clock at the destination node of an ATM network; and

FIG. 4 are timing diagrams showing the gating function at the apparatus of FIG. 3.

DETAILED DESCRIPTION

The concept of the Residual Time Stamp is described with reference to FIG. 1. In FIG. 1, and in the description hereinafter, the following terminology is used:

f_n—network clock frequency, e.g. 155.52 MHz;

f_{nx}—derived network clock frequency,

$$f_{nx} = \frac{f_n}{x},$$

where x is a rational number;

f_s—service clock frequency;

N—period of RTS in units of the service clock (f_s) cycles;

T_n—the n-th period of the RTS in seconds;

±ε—tolerance of the source clock frequency in parts per million;

M_n (M_{nom}, M_{max}, M_{min})—number of f_{nx} cycles within the n-th (nominal, maximum, minimum) RTS period, which are, in general, non-integers.

As can be noted in FIG. 1, during the n-th period, T_n, corresponding to N service clock cycles, there are M_n network derived clock cycles. As aforenoted, since the service clock and the network clock are neither synchronized nor integrally related in frequency, this number of derived network clock cycles is not an integer. Since all practical timing recovery techniques transmit only integer values, the fractional part of M_n must be dealt with. Simple truncation or rounding of the fractional part in each RTS time slot is not permissible, as this would lead to a "random walk" type error accumulation. Rather, it is necessary to accumulate the fractional parts at the transmitter and use the accumulated value to modify the transmitted integer quantity. Since it is most convenient to generate RTS by an asynchronous counter, as will be described hereinafter in conjunction with the description of FIG. 2, a "truncation" operation is natural, reflecting the fact that an asynchronous counter's output does not change until the subsequent input pulse arrives. To formalize these notions, S_n is defined as the truncated value of M_n after accounting for the left over fractional part, d_n, from the (n−1)-th interval, viz.,

$$S_n=\lfloor M_n+d_n \rfloor \quad (1)$$

and

$$d_{n+1}=d_n+M_n-S_n \quad (2)$$

where $\lfloor a \rfloor$ denotes the largest integer less than or equal to a. Since for accurate clocks, the range of M_n, is very tightly constrained, i.e., $M_{max}-M_{min}=2y<M_n$, the variation in S_n is also smaller than its magnitude. It follows from Equation (1) that

$$\lfloor M_{min}+d_n \rfloor \geqq S_n \geqq \lfloor M_{max}+d_n \rfloor \quad (3)$$

Since the maximum and minimum of d_n are 1 and 0 respectively, S_n is bounded by,

$$\lfloor M_{min} \rfloor \geqq S_n \geqq \lfloor M_{max} \rfloor+1 \quad (4)$$

This implies, that the most significant portion of S_n carries no information and it is necessary to transmit only its least significant portion. This, therefore, is the essential concept of the RTS. The minimum resolution required to represent the residual part of S_n unambiguously is a function of N, the ratio of the network derived frequency to the service frequency, and the service clock tolerance, ±ε. The maximum deviation, y, between the nominal number of derived network clock pulses in an RTS period, M_{nom}, and the maximum or minimum values of M (M_{max} or M_{min}) is given by,

$$y = N \times \frac{f_{nx}}{f_s} \times \varepsilon \quad (5)$$

where M_{nom} equals

$$N \times \frac{f_{nx}}{f_s}.$$

A specific numerical example can be considered for clarity of understanding. As illustrative derived network clock frequency and service clock frequencies could be given by f_{nx}=155.52 MHZ (for x=1), and f_s=78.16 MHz (nominal), respectively. A typical RTS sampling period (N) is 3008, which corresponds to a period of 8 cells and a 47-octet payload per cell (47 bytes/cell×8 bits/byte×8 cells per RTS period). Using these numbers, M_{nom}=5985.2119. If it is further reasonable to assume that the service clock tolerance is 200 parts per million, i.e., ±200×10^{-6}. From equation (5), therefore, y=1.197, which demonstrates that it is superfluous to transmit the full S_n in each RTS sampling period and transmission of the last few (P) bits of S_n is sufficient. This P-bit sample is the Residual-TS (RTS).

FIG. 2 is a block diagram of the source node of an ATM network showing apparatus for generating and transmitting the RTS. The basic network clock, C, shown at 10, serves as the reference for timing of all nodes of the synchronous network being here considered. This clock, having a frequency f_n, is divided in frequency by a rational factor x by a divider 11 to produce a derived network clock having a frequency f_{nx}. Preferably, x would be an integer value. The dividing factor is chosen so that the P bits available can unambiguously represent the number of derived network clock cycles within an RTS period. In the case where

$$\frac{f_{nx}}{f_s}$$

is less than or equal to two, as in the example above, it can be shown that a 3-bit RTS is sufficient.

The derived network clock, f_{nx}, drives a P-bit counter, which is continuously counting these derived network clock pulses, modulo 2^P. The service clock, f_s, on lead 13, which is derived from the service data signal (not shown) to be transmitted over the ATM network, is divided in frequency by N, the desired RTS period in units of f_s cycles, by divide-by N circuit 14. As shown in FIG. 2, the output of divider 14 is a pulse signal in which T_n is its n-th period. At every T seconds (N source clock cycles) latch 15 samples the current count of counter 12, which is then the P-bit RTS to be transmitted. As aforedescribed, this number represents the residual part of S_n and is all that is necessary to be transmitted to recover the source clock at the destination node of the network.

Each successive RTS is incorporated within the ATM adaptation layer overhead by AAL processor 16. The associated data to be transmitted (not shown) is also processed by processor 16 to form the payload of the cells, which are then assembled by an ATM assembler 17, which adds an ATM header for transmission over the network 18.

With reference again to the previous example, a four-bit counter (P=4) can be assumed to be used. Since M_{nom}=5985.2119 and 5985.2119 (modulo 16)=1.2119, a typical RTS output sequence when the source is at nominal frequency will be as follows;

. . . 5,6,7,9,10,11,12,13,15,1,2, . . .

Since the counter 16, in effect, quantizes by truncation, the RTS changes only by integer values. The changes in RTS are

such that their average is exactly equal to M_{nom} (modulo 2^P). In this example, the changes are either 1 or 2 with the change of 2 occurring either every 4 or 5 RTSs in such a way that the average interval is 1/0.2119=4.7198. In general, successive RTSs are related by

$$RTS_{n+1}=RTS_n+S_n=RTS_n+[d_n+M_n](\text{modulo } 2^P) \tag{6}$$

In order to guarantee that no information is lost due to the modulo arithmetic, i.e., that the transmitted RTS represents S_n unambiguously, it can be seen from equation (4) that the number of bits used for transmission must satisfy:

$$2_P \geq [M_{max}]-[M_{min}]+2 \tag{7}$$

Thus, in the example above, the number of bits allocated to the RTS must be 3 or greater. It can be noted that the number of bits necessary to unambiguously represent the number of derived network clock cycles within the RTS period is substantially less than the number of bits that would be required to represent the absolute number of clock cycles within the same interval. In the example above, for example, a 13-bit number would be required to represent M_{nom}.

If equation (7) is satisfied, knowledge of M_{nom} in the receiver at the destination node along with the received RTSs can be used to reproduce the service clock from the synchronous network clock. FIG. 3 shows one receiver implementation for reproducing the service clock from the received RTSs. At the receiver the common network clock 10 is available as it was at the transmitter. As in the transmitter, a divider 31 divides the network clock frequency, f_n by the same factor of x as divider 11 in the source node, to produce the same derived network clock signal having a frequency f_{nx} as was used by the transmitter at the source node of FIG. 2.

In a structure paralleling the transmitter in FIG. 2, a disassembler 32 processes the ATM headers received from the network 18 and passes the payload to an AAL processor 33. In addition to extracting the transmitted data (not shown), processor 33 extracts the periodic transmitted RTSs, which are sequentially stored in a FIFO 34, which is used to absorb the network cell jitter. The earliest received RTS in FIFO 34 is compared by P-bit comparator 35 with the count of a free running P-bit counter 36, driven by the derived network clock, f_{nx}. Whenever the output of counter 36 matches the current RTS, comparator 35 generates a pulse. Since counter 36 is a modulo 2_P counter, the RTS in FIFO 34 matches the count of counter 36 every 2_P derived network clock pulses, f_{nx}. The output of comparator 35 thus consists of a train of pulses that are separated, except for the first pulse, by 2_P cycles of the derived network clock. In order to select the output pulse of comparator 35 that corresponds to the end of the fixed period of the transmitted service clocks, which is the period per RTS to be recovered, gating circuitry 37 is employed. Gating circuitry 37, which includes a counter 38, a gating signal generator 39, and an AND gate 40, gates only that pulse output of comparator 35 produced after counting, from the last gated output pulse, a minimum number, M_l, of derived network clock cycles. This minimum number, M_l, is given by:

$$M_l=[M_{nom}]-^{(P-1)} \tag{8}$$

This ensures that $[M_{max}]-2_P<M_l<[M_{min}]$, and thus the gating pulse is guaranteed to select the correct RTS.

The gating function is best explained in conjunction with the timing diagrams of FIG. 4. Initially, it can be assumed

that gating signal generator 39 is set to keep AND gate 40 open. Comparator 35 compares the first RTS in FIFO 34 with the free-running count of counter 36. When the count of counter 36 matches this first RTS, shown in FIG. 4 as "2", comparator 35 produces a pulse which is gated through AND gate 40. This gated output pulse resets gating signal generator 39 thereupon turning off AND gate 40, resets the counter of counter 38 to zero, and reads the next stored RTS, "5", in FIFO 34. When counter 36 reaches the count of "5", comparator 35 produces another output pulse. AND gate 40, however, is OFF and remains off until counter 38 counts M_l derived network clock cycles. Therefore, as noted in FIG. 4, all the subsequent matches of the RTS, "5" and the count of counter 36, which occur every 2_P derived network clock cycles, are blocked by AND gate 40. These subsequent pulses are blocked until counter 38 reaches a count of that minimum number of clock cycles that can comprise the fixed interval to be recovered from the RTS. After counting M_l derived network clock cycles, counter 38 generates a pulse which signals gating signal generator 39 to open AND gate 40. The next pulse produced by comparator 35 upon the match between the RTS in FIFO 34 and the count of counter 36 is gated through AND gate 40. This pulse, as before, resets counter 38, resets gating signal generator 39, and reads-in the next stored RTS to the output of FIFO 34. The resultant time difference between output pulses of AND gate 40 is the desired fixed time interval, S_n, to be recovered from the transmitted RTSs. As previously defined in equation (1), S_n is the truncated value in the nth interval, after accounting for a left over portion from the (n−1)-th interval, of the actual number of derived network clock cycles within the fixed interval defined by N source clock cycles. As can be noted, S_n modulo (2^P) is equal to the difference of the RTSs associated with the pulses matched by comparator 35 right before and right after the reset. Thus in FIG. 4, for the n-th period, this is the difference between "5" and "2", or "3", and for the (n+1)-st period, this is the difference between "9" and "5" or "4". The resultant pulse train at the output of gating circuitry 37 can be seen to duplicate the signal at the source node of the network, which is defined by N service clock cycles, as modified by the quantization effect of the RTSs. This pulse stream is input to a multiply-by N phase-locked loop 41 which multiplies the frequency by the factor of N and smooths out the variation of the reproduced periods. The resultant output clock signal, f_s, is the reproduced service timing signal, which can be employed by the circuitry at the destination node.

The above-described embodiment is illustrative of the principles of the present invention. Other embodiments could be devised by those skilled in the art without departing from the spirit and scope of the present invention.

What is claimed is:

1. A method of recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising the steps of:

(a) at the source node, dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

(b) at the source node, counting the network clock cycles modulo 2^P, where 2_P is less than the number of network clock cycles within an RTS period and P is chosen so that the 2_P counts uniquely and unambiguously represent the range of possible network clock cycles within an RTS period;

(c) transmitting from the source node to the destination node an RTS at the end of each RTS period that is equal to the modulo 2_P count of network clock cycles at that time;

(d) determining from the RTSs received at the destination node, the number of network clock cycles in each RTS period;

(e) generating a pulse signal from the network clock at the destination node in which the period between each pulse in the pulse signal equals the determined number of network clock cycles in the corresponding RTS period; and

(f) multiplying the frequency of the pulse signal generated in step (e) by the same factor of an integer N used in step (a) to recover the timing clock of the service input.

2. The method of claim 1 wherein the network clock frequency is less than or equal to twice the service clock frequency.

3. A method of recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising the steps of:

(a) at the source node, dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

(b) at the source node, dividing the network clock by a rational factor to form a derived network clock;

(c) at the source node, counting the derived network clock cycles modulo 2^P, where 2_P is less than the number of derived network clock cycles within an RTS period and P is chosen so that the 2_P counts uniquely and unambiguously represent the range of possible derived network clock cycles within an RTS period;

(d) transmitting from the source node to the destination node an RTS at the end of each RTS period that is equal to the modulo 2_P count of derived network clock cycles at that time;

(e) at the destination node, dividing the network clock by the same rational factor used at the source node to form a derived network clock equal to the derived network clock at the source node;

(f) determining from the RTSs received at the destination node, the number of derived network clock cycles in each RTS period;

(g) generating a pulse signal from the derived network clock at the destination node in which the period between each pulse in the pulse signal equals the determined number of derived network clock cycles in the corresponding RTS period; and

(h) multiplying the frequency of the pulse signal generated in step (g) by the same factor of an integer N used in step (a) to recover the timing clock of the service input.

4. The method of claim 3 wherein the derived network clock frequency is less than or equal to twice the service clock frequency.

5. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising at the source node:

dividing means for dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

counting means connected to the network clock for counting network clock cycles modulo 2^P, where 2_P is less than the number of network clock cycles within an RTS period and P is chosen so that the 2_P counts uniquely and unambiguously represent the range of possible network clock cycles within an RTS period; and

transmitting means, responsive to the RTS periods formed by said dividing means and the count of said counting means, for transmitting over the telecommunications network an RTS at the end of each RTS period that is equal to the modulo 2^P count of network clock cycles at that time;

and comprising at the destination node:

receiving means for receiving the RTSs transmitted over the telecommunications network by said transmitting means;

converting means responsive to the received RTSs and the network clock for converting the received RTSs into a pulse signal in which the periods between pulses are determined from the numbers of network clock cycles associated with the counts of network clock cycles within said RTS periods; and

means for multiplying the frequency of the pulse signal generated by said converting means by the same factor of an integer N used in said dividing means for recovering the timing clock of the service input.

6. Apparatus in accordance with claim 5 wherein the network clock frequency is less than or equal to twice the service clock frequency.

7. Apparatus in accordance with claim 5 wherein said converting means comprises:

means for sequentially storing the received RTSs;

means for counting network clock cycles modulo 2_P;

comparing means for comparing the modulo 2_P count of network clock cycles with a stored RTS and for generating a pulse each time the count of network clock cycles matches the RTS; and gating means for gating to said multiplying means, for each sequentially received and stored RTS, the pulse produced by said comparing means that occurs after the counting means counts, starting-in-time from the previous gated pulse, a number of network clock cycles that is greater than a predetermined minimum absolute number of network clock cycles that can occur within any RTS period.

8. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising at the source node:

first dividing means for dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

second dividing means for dividing the network clock by a rational factor to form a derived network clock;

counting means connected to the network clock for counting derived network clock cycles modulo 2^P, where 2_P is less than the number of derived network clock cycles within an RTS period and P is chosen so that the 2_P counts uniquely and unambiguously represent the range of possible derived network clock cycles within an RTS period; and

transmitting means, responsive to the RTS periods formed by said first dividing means and the count of said counting means, for transmitting over the telecommu-

nications network an RTS at the end of each RTS period that is equal to the modulo 2^P count of derived network clock cycles at that time;

and comprising at the destination node:

receiving means for receiving the RTSs transmitted over the telecommunications network by said transmitting means;

means for dividing the network clock by the same rational factor used at the source node to form a derived network clock;

converting means responsive to the received RTSs and the derived network clock for converting the received RTSs into a pulse signal in which the periods between pulses are determined from the numbers of derived network clock cycles associated with the counts of derived network clock cycles within said RTS periods; and

means for multiplying the frequency of the pulse signal generated by said converting means by the same factor of an integer N used in said first dividing means for recovering the timing clock of the service input.

9. Apparatus in accordance with claim 8 wherein the derived network clock frequency is less than or equal to twice service clock frequency.

10. Apparatus in accordance with claim 8 wherein said converting means comprises:

means for sequentially storing the received RTSs;

means for counting derived network clock cycles modulo 2_P;

comparing means for comparing the modulo 2_p count of derived network clock cycles with a stored RTS and for generating a pulse each time the count of derived network clock cycles matches the RTS; and

gating means for gating to said multiplying means, for each sequentially received and stored RTS, the pulse produced by said comparing means that occurs after the counting means counts, starting-in-time from the previous gated pulse, a number of derived network clock cycles that is greater than a predetermined minimum absolute number of derived network clock cycles that can occur within any RTS period.

11. Apparatus for generating a representation of the relationship between the timing clock of a service input, at a source node of a packet-based telecommunications network, and a network clock, the apparatus comprising:

(a) means, at the source node, for defining a residual time stamp (RTS) period as an integral number N of source-node service clock cycles;

(b) means, at the source node, for defining a derived network clock frequency f_{nx} from a network frequency f_n where $f_{nx}=f_n/x$, x is a rational number, and f_{nx} is less than or equal to twice the service clock frequency;

(c) means, at the source node, for counting the derived network clock cycles modulo 16 in an RTS period and;

(d) means for transmitting from the source node an RTS that is equal to the modulo 16 count of derived network clock cycles in the RTS period.

12. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of the packet-based telecommunications network, wherein the destination and source nodes have a common network clock divided network clock and wherein the service node generates a residual time stamp (RTS) signal equal to a modulo 16 count of cycles based on the network clock; the apparatus comprising:

means for receiving the RTS signal;

means for determining the number of network cycles in an RTS period from the RTS signal; and

means responsive to the determining means for generating a clock signal which represents a recovery of the timing clock of the service input.

13. Apparatus for generating a representation of a timing clock of a service input at a source node of a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source node and a destination node; the apparatus comprising:

(a) means for defining a time interval by a fixed number of service clock cycles; and

(b) means for generating a digital representation of a quantized difference between an actual number of network clock cycles within the time interval and an expected number of network clock cycles within the time interval, the difference being within a defined time window corresponding to a frequency variation of the source-node service clock.

14. The apparatus of claim 13, wherein the digital representation represents a chosen number of the least significant bits of the quantized actual number, the chosen number being sufficient to represent a range of frequency deviations of the source-node service clock variation.

15. The apparatus of claim 14 wherein the chosen number is 4.

16. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said network, wherein a common network clock or divided network clock is provided for the destination node and the source node and a time interval is defined by a fixed rational number of source-node service clock cycles; the apparatus comprising:

means for receiving generating a digital representation of a quantized difference between an actual number of network clock cycles within the time interval and an expected number of network clock cycles within the time interval, the difference being within a defined time window corresponding to a frequency variation of the source-node service clock; and

means for recovering the source-node service clock at the destination node by constructing a timing signal at the destination node based on a received representation of the network cycle difference.

17. Apparatus for reconstructing, at a destination node of a packet-based telecommunications network, a timing clock of a service input at a source node of the network, wherein a common network clock or divided network clock is provided for the destination node and the source node and wherein the reconstruction is based on successive modulo 2^P numerical representations of the number of network clock cycles within corresponding successive predetermined time periods, each of the numerical representations being received from the source node and being less than the actual number of network clock cycles within its corresponding time period; the apparatus comprising:

means for receiving the numerical representations in succession at the destination node;

means for converting the received numerical representations into successive fixed time intervals, wherein each successive interval corresponds to the number of network clock cycles in a corresponding one of the predetermined time periods; and

means for recovering the source-node service clock from the fixed time intervals.

18. The apparatus of claim 17, wherein the converting means further comprises:

means for sequentially storing the successive modulo 2^P numerical representations;

means for comparing the successive numerical representations with a modulo 2^P count of the network clock cycles at the destination node to generate a comparison signal for each match between the numerical representation and the modulo 2^P count at the destination node; and

means for successively selecting a proper comparison signal by waiting until a minimum number of network clock cycles has occurred.

19. A method for generating a signal at a source node for use in recovering a source-node service clock at a destination node in a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source and destination nodes; the steps of the method comprising:

defining a time interval by a fixed number of cycles of the source-node service clock;

determining an actual number of cycles of the network clock within the time interval;

determining a numerical deviation of the number of actual network clock cycles from another number of network clock cycles that would occur if the source-node service clock frequency were nominal; and

generating a digital signal representing the numerical deviation for transmission through the network to the destination node.

20. A method for recovering a source-node service clock at a destination node in a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source and destination nodes, wherein an actual time interval is defined by a fixed number of cycles of the source-node service clock, and wherein a number of actual cycles of the network clock within the actual time interval and a numerical deviation of the number of actual network clock cycles from another number of network clock cycles known nominally to be within the time interval are determined; the steps of the method comprising:

receiving a digital signal representing the numerical deviation transmitted through the network from the source node; and

generating a timing signal corresponding to the source-node service clock on the basis of the digital signal representing the numerical deviation.

21. A method for recovering, at a destination node of a packet-based telecommunications network, a timing clock of a service input at a source node of the packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the destination node and the source node; the steps of the method comprising:

defining a time interval by a fixed number of cycles of the source-node service clock;

determining an actual number of cycles of the network clock within the time interval;

determining a numerical deviation of the number of actual network clock cycles from another number of network clock cycles that would occur within the time interval if the source-node service clock frequency were nominal;

generating a digital signal representing the numerical deviation;

transmitting the digital signal to the destination node; and

generating a timing signal at the destination node corresponding to the source node service clock on the basis of the digital signal and a signal from the network clock.

22. The method of claim 21 wherein the numerical deviation is determined as a function of the fixed number of source-node service clock cycles, the frequencies of the network clock and the source-node service clock, and a frequency variation of the source-node service clock.

23. The method of claim 21 further including the step of employing a modulo 2^P counter to generate a representation of the numerical deviation.

24. Apparatus for generating a signal at a source node for use in recovering a source-node service clock at a destination node in a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source and destination nodes; the apparatus comprising:

means for defining a time interval by a fixed number of cycles of the source-node service clock;

means for determining a number of actual cycles of the network clock within the time interval;

means for determining a numerical deviation of the number of actual network clock cycles from another number of network clock cycles that would occur within the time interval if the source-node clock frequency were nominal; and

means for generating a digital signal representing the numerical deviation for transmission through the network to the destination node.

25. The apparatus of claim 24 wherein the numerical deviation is determined as a function of the fixed number of source-node service clock cycles, and frequencies of the network clock and the source-node service clock, and a nominal frequency of the source-node service clock.

26. The apparatus of claim 24 wherein the numerical deviation determining means includes a modulo 2^P counter which generates the numerical deviation.

27. The apparatus of claim 26 wherein a value of 2^P is 16.

28. Apparatus for recovering a source-node clock at a destination node in a packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the source and destination nodes and wherein a time interval is defined by a fixed number of cycles of the source-node service clock, and wherein a number of actual cycles of the network clock within the time interval and a numerical deviation of the number of actual network clock cycles from another number of network clock cycles that would occur within the time if the source-node service clock frequency were nominal;

means for receiving a digital signal representing the numerical deviation transmitted through the network from the source node; and

means for generating a timing signal corresponding to the source-node service clock on the basis of the digital signal representing the numerical deviation.

29. Apparatus for recovering, at a destination node of a packet-based telecommunications network, a timing clock of a service input at a source node of the packet-based telecommunications network, wherein a common network clock or divided network clock is provided for the destination node and the source node; the apparatus comprising:

means for defining a time interval by a fixed number of cycles of the source-node service clock;

means for determining a number of actual cycles of the network-clock within the time interval;

means for determining a numerical deviation of the number of actual network clock cycles from another number of network clock cycles that would occur within the time interval if the source-node service clock frequency were nominal;

means for generating a digital signal representing the numerical deviation;

means for transmitting the digital signal to the destination node; and

means for generating a timing signal at the destination node corresponding to the source-node service clock on the basis of the digital signal and a signal from the network clock.

30. The apparatus of claim 29 wherein the numerical deviation is determined as a function of the fixed number of source-node service clock cycles, frequencies of the network clock and the source-node service clock, and a nominal frequency of the source-node service clock.

31. The apparatus of claim 29 wherein the numerical deviation determining means includes a modulo 2^P counter which generates the numerical deviation.

32. The apparatus of claim 29 wherein means are provided for carrying any fractional network cycle in any time interval for network cycle counting by the modulo 2^P counter for counting the next time interval.

33. A method for generating a representation of the relationship between the timing clock of a service input, at a source node of a packet-based telecommunications network, and a network clock, the method comprising the steps of:

(a) defining, at the source node, a residual time stamp (RTS) period as an integral number N of source-node service clock cycles;

(b) defining, at the source node, a derived network clock frequency f_{nx} from a network frequency f_n where $f_{nx}=f_n/x$, x is a rational number, and f_{nx} is less than or equal to twice the service clock frequency;

(c) counting, at the source node, the derived network clock cycles modulo 16 in an RTS period; and

(d) transmitting from the source node an RTS that is equal to the modulo 16 count of derived network clock cycles in the RTS period.

* * * * *

EXHIBIT B

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United States Patent [19]

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Fleischer et al.

[54] **SYNCHRONOUS RESIDUAL TIME STAMP FOR TIMING RECOVERY IN A BROADBAND NETWORK**

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[52] **U.S. Cl.** **375/106**; 375/111; 375/113

[58] **Field of Search** 370/100.1, 94.2, 94.1; 375/106, 107, 110, 110, 113, 118

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,961,188 10/1990 Lau 370/94.2

OTHER PUBLICATIONS

"Jitter Reduction in ATM Networks," Julio Gonzales and Jean-Paul Le Meur Proceedings ICC '91, 9.4.1–9.4.6.

"Jitter and Clock Recovery for Periodic Traffic in Broadband Packet Networks," R. P. Singh, S. H. Lee and C. K. Kim, Presented at IEEE Globecom '88, Florida, Dec. 1988.

"Adaptive Clock Synchronization for Real-Time Traffic in Broadband Packet Networks" R. P. Singh and S. H. Lee, Presented-8th Eur. Conf. on Electrotechnics, Stockholm, Sweden, Jun. 1988.

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[57] **ABSTRACT**

A Residual Time Stamp (RTS) technique provides a method and apparatus for recovering the timing signal of a constant bit rate input service signal at the destination node of a synchronous ATM telecommunication network. At the source node, a free-running P-bit counter counts cycles in a common network clock. At the end of every RTS period formed by N service clock cycles, the current count of the P-bit counter, defined as the RTS, is transmitted in the ATM adaptation layer. Since the absolute number of network clock cycles likely to fall within an RTS period will fall within a range determined by N, the frequencies of the network and service clocks, and the tolerance of the service clock, P is chosen so that the 2^P possible counts, rather than representing the absolute number of network clock cycles an RTS period, provide sufficient information for unambiguously representing the number of network clock cycles within that predetermined range. At the destination node, a pulse signal is derived in which the periods are determined by the number of network clock cycles represented by the received RTSs. This pulse signal is then multiplied in frequency by N to recover the source node service clock.

10 Claims, 3 Drawing Sheets

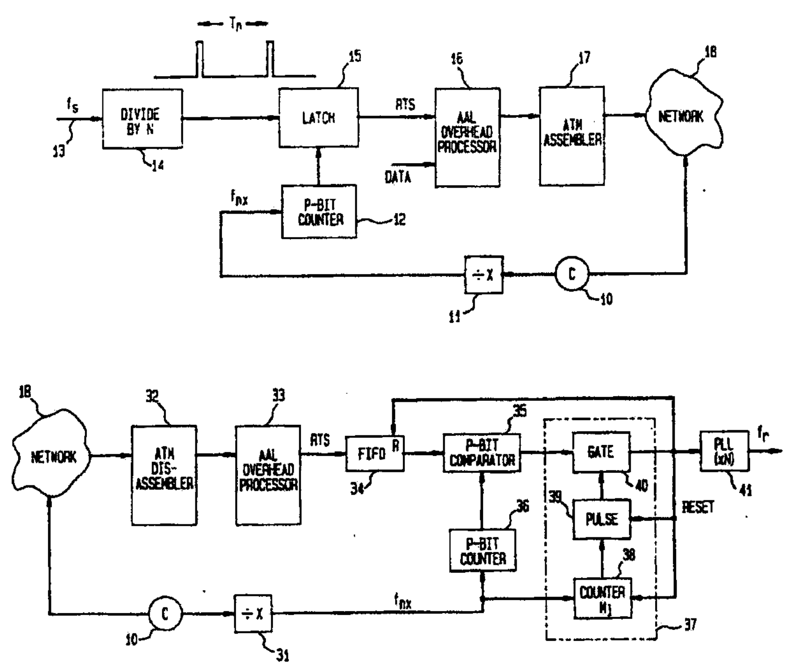

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FIG. 1

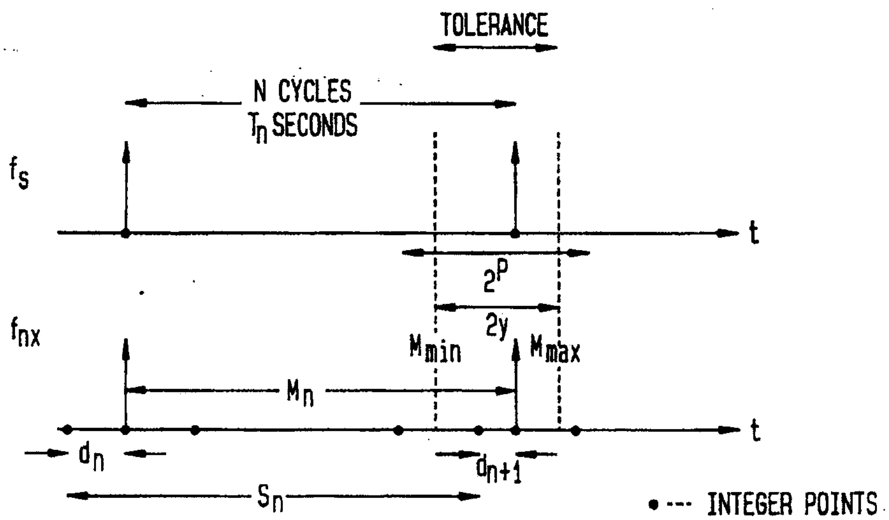

TOLERANCE
N CYCLES
T_n SECONDS
f_s
t
2^P
f_{nx}
2y
M_{min}
M_{max}
M_n
t
d_n
d_{n+1}
S_n
• --- INTEGER POINTS

FIG. 4

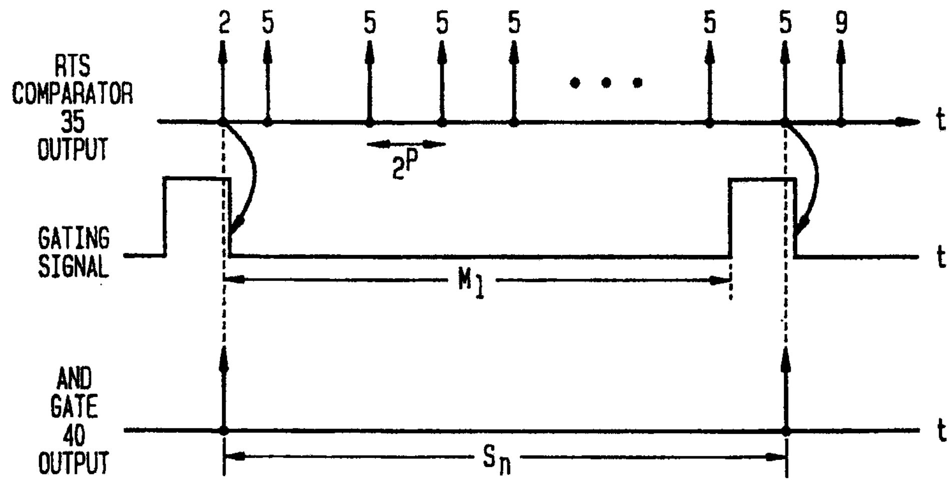

2 5 5 5 5 5 5 9
RTS COMPARATOR 35 OUTPUT
t
2^P
GATING SIGNAL
t
M_1
AND GATE 40 OUTPUT
t
S_n

FIG. 2

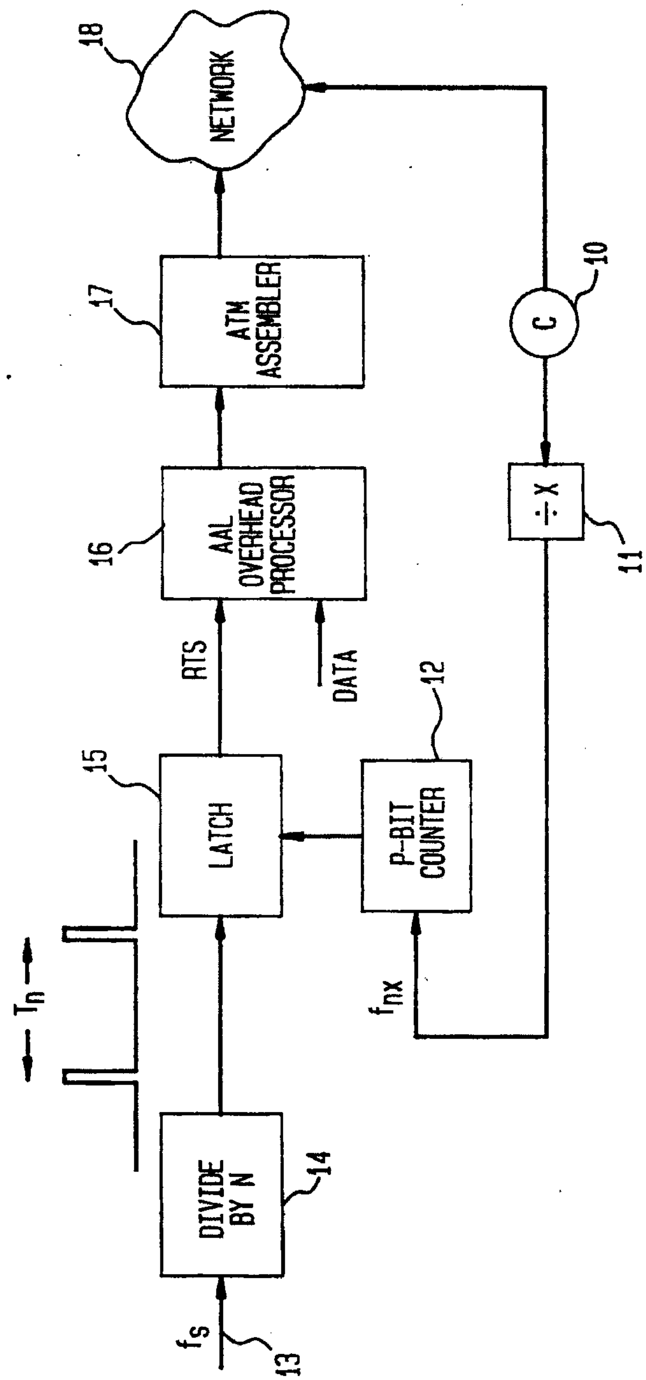
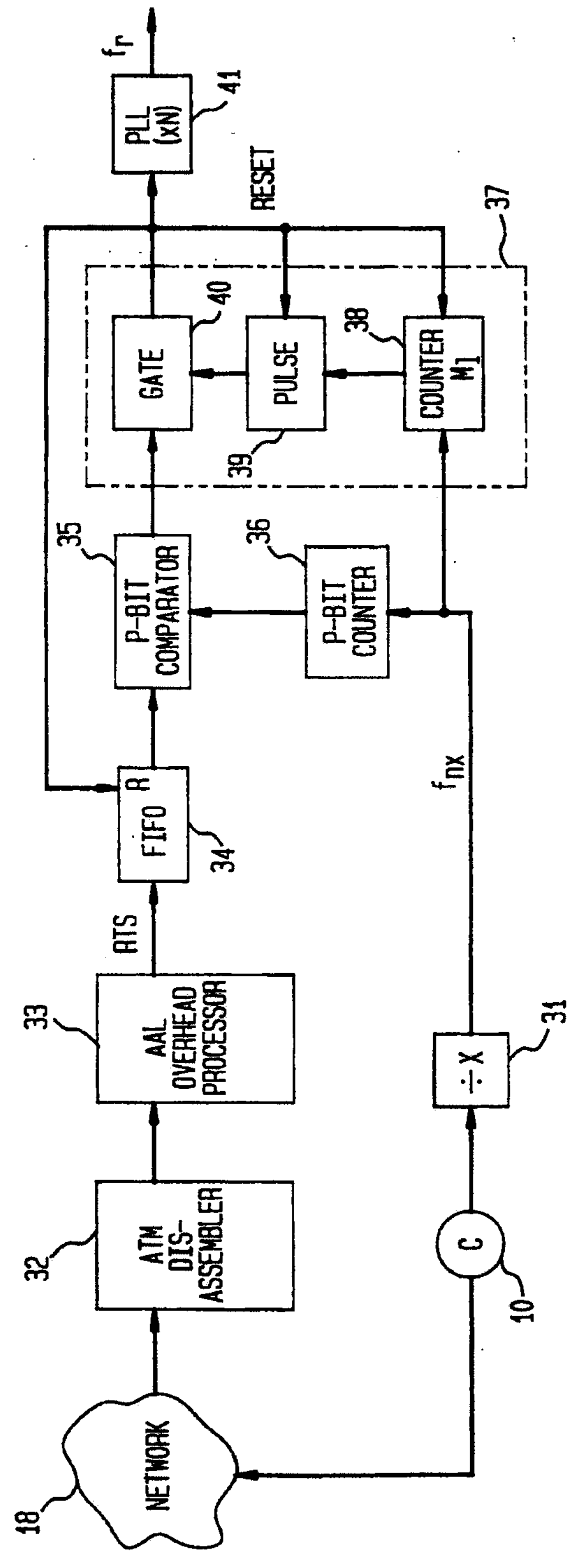

NETWORK
18
ATM ASSEMBLER
17
AAL OVERHEAD PROCESSOR
16
RTS
DATA
LATCH
15
P-BIT COUNTER
12
DIVIDE BY N
14
f_s
13
T_n
f_{nx}
C
10
÷ X
11

FIG. 3



NETWORK
18
ATM DIS- ASSEMBLER
32
AAL OVERHEAD PROCESSOR
33
RTS
FIFO
R
34
P-BIT COMPARATOR
35
P-BIT COUNTER
36
GATE
40
PULSE
39
COUNTER M_1
38
37
RESET
PLL (xN)
41
f_r
f_{nx}
÷X
31
C
10

SYNCHRONOUS RESIDUAL TIME STAMP FOR TIMING RECOVERY IN A BROADBAND NETWORK

BACKGROUND OF THE INVENTION

This invention relates to timing recovery of a source node service clock frequency at a destination node in a broadband asynchronous transfer mode (ATM) network where the source and destination nodes receive reference timing signals derived from a single master clock.

Asynchronous Transfer Mode (ATM) is a packet oriented technology for the realization of a Broadband Integrated Services Network (BISDN). By using ATM, network resources can be shared among multiple users. Moreover, various services including voice, video and data can be multiplexed, switched, and transported together under a universal format. Full integration will likely result in simpler and more efficient network and service administration and management. However, while conventional circuit-switching is optimized for real-time, continuous traffic, ATM is more suitable for the transport of bursty traffic such as data. Accommodation of constant bit rate (CBR) services is, however, an important feature of ATM, both for universal integration and for compatibility between existing and future networks. In the transport of a CBR signal through a broadband ATM network, the CBR signal is first segmented into 47-octet units and then mapped, along with an octet of ATM Type I Adaptation Layer (AAL) overhead, into the 48-octet payload of the cell. The cells are then statistically multiplexed into the network and routed through the network via ATM switches.

It is essential to the proper delivery of such CBR service traffic in a broadband network that the clock controlling the destination node buffer be operating at a frequency precisely matched to that of the service signal input at the source node in order to avoid loss of information due to buffer over- or under-flow. However, unlike the circuit-switched transport of service data wherein the clock frequency at the destination node may be traced directly back to that of the source node by the regular, periodic arrival of the CBR traffic, transport in an ATM network inherently results in cell jitter, i.e. the random delay and aperiodic arrival of cells at a destination node, which essentially destroys the value of cell arrival instances as a means for directly recovering the original service signal input frequency.

Such cell jitter, generally the result of the multiplexing of transport cells in the broadband network and the cell queuing delays incurred at the ATM switches in the network, is substantially unpredictable. Thus, little is known about the cell arrival time beyond the fact that the average cell delay is a constant, assuming that the ATM network provides sufficient bandwidth to ensure against loss of cells within the network. As a means for closely approximating the service signal frequency at the destination node, some consideration had previously been given to utilizing a direct extension of circuit-switched timing recovery practices which rely entirely upon a buffer fill signal as the basis for recovery of the source timing. However, due to the lack of knowledge of statistics of the cell jitter, this approach would have required a phase-locked loop with very low cut-off frequency (in the order of a few Hz) and would thus

have resulted in excessive converging time and degradation of jitter and wander performance.

A number of schemes have been proposed to improve upon such a conventional manner of recovering service timing in the presence of cell jitter, yet none has achieved this end economically and without extensive control systems of notable complexity. Singh et al., for example, in "Adaptive Clock Synchronization Schemes For Real-Time Traffic In Broadband Packet Networks," 8th European Conference on Electrotechnics, Stockholm, Sweden, June 1988, and "Jitter And Clock Recovery For Periodic Traffic In Broadband Packet Networks," IEEE Globecom '88, Florida, December 1988, have proposed algorithms which attempt to more closely estimate cell jitter statistics and derive timing recovery from those indications. These adaptive approaches, suggested to be applicable to both synchronous and non-synchronous networks, rely upon the interaction of increasingly complex algorithms which would require the noted extensive controls for implementation.

These prior art schemes described above can be classified as non-synchronous techniques, which are based on the simple fact that the expected value of the network cell jitter is zero and thus rely on phase filtering. Synchronous techniques, on the other hand, utilize the fact that common timing is available at both the transmitter and the receiver. In a synchronous broadband ATM network, such as the Synchronous Optical Network (SONET) prescribed by American National Standard, ANSI T1.105-1988, "Digital Hierarchy Optical Interface Rates and Formats Specification," Mar. 10, 1988, the network source and destination node control clocks are synchronized to the same timing reference. As a result, there is no necessity for relying upon any extraneous phenomenon such as instants of cell arrival to provide a datum base for determining the relative frequencies of those control clocks. The effect of cell jitter caused by multiplexing and switching delays in the network is therefore of little consequence in any procedure for circuit transporting CBR service, which is based, as is the present invention, on an actual synchrony of node timing. Thus being devoid of concern for cell jitter, this process is free to simply determine the difference in frequency between the CBR service signal input at the source node and the source/destination node timing clock(s).

U.S. Pat. No. 4,961,188 issued on Oct. 2, 1990 to Chi-Leung Lau, co-inventor herein, discloses a synchronous frequency encoding technique (SFET) for clock timing in a broadband network. The SFET takes advantage of the common timing reference at both the source and the receiver. At the source, the asynchronous service clock is compared to the network reference clock. The discrepancy between properly chosen submultiples of the two clocks is measured in units of a preassigned number of slip cycles of network clock. This clock slip information is conveyed via a Frequency Encoded Number (FEN) which is carried in the ATM Adaptation Layer (AAL) overhead. At the receiver, the common network clock and the FEN are used to reconstruct the service clock. This timing recovery process does not rely on any statistics of the cell jitter except that it has a known, bounded amplitude. Therefore, the recovered clock has jitter performance comparable to that of the circuit-switched network.

An alternative proposed approach is known as Time Stamp (TS). In the Time Stamp approach (see, for ex-

ample, Gonzales et al, "Jitter Reduction in ATM Networks", Proceedings ICC'91, 9.4.1–9.4.6), the network clock is used to drive a multi-bit counter (16-bits in the proposal), which is sampled every fixed number of generated cells (e.g., 16). Thus, a fixed number, N, of service clocks cycles is used as the measuring yardstick. The sampled value of the 16-bit counter is the TS that inherently conveys the frequency difference information. Because of the size of the TS (2 octets), it has been proposed that the TS be transmitted via the Convergence Sublayer (CS) overhead. Thus the TS is a 16-bit binary number occurring once every N service clock cycles. Differences in successive TSs represent the quantized values of M, where M is the number of network clock cycles during the fixed TS period. At the receiver, the TS period is reconstructed from the received TSs and the network clock. A free-running 16-bit counter is clocked by the network clock and the output of the counter is compared to the received TSs which are stored in a TS FIFO. A pulse is generated whenever there is a match between the TS and the 16-bit counter. The service clock is recovered by supplying the resultant pulse stream as the reference signal to a multiply-by-N phase locked loop (PLL).

A comparison of the SFET approach and the TS approach reveals advantages and disadvantages for each. In the SFET approach there is a relatively stringent requirement on the derived network clock since it must be slightly larger than the service clock. Advantageously, however, a convergence sublayer is not required to transmit the FEN and only small overhead bandwidth is required to transmit the necessary information. On the other hand, the TS approach is more flexible in that it does not require stringent relationships between the service clock and the network derived clock and can therefore support a range of service bit rates. Disadvantageously, however, a rigid convergence sublayer structure is required to transmit the TS, which adds complexity and makes inefficient use of the overhead bandwidth.

An object of the present invention is to achieve synchronous timing recovery with an approach that has the advantages of both the SFET and TS approaches, specifically, the efficiency of SFET and the flexibility of TS.

SUMMARY OF THE INVENTION

As described hereinabove, the TS approach requires a large number of bits (16-bits in the example), to represent the number of network clock cycles within a time interval defined by a fixed number (N) of service clock cycles. In accordance with the present invention, the number of bits required to represent the number of network clock cycles within that time interval is substantially reduced. This is possible through the realization that the actual number of network clock cycles, M (where M is not necessarily an integer), deviates from a nominal known number of cycles by a calculable deviation that is a function of N, the frequencies of the network and service clocks, and the tolerance of the service clock. Specifically, therefore, rather than transmitting a digital representation of the quantized actual number of network clock cycles within the interval, only a representation of that number as it exists within a defined window surrounding an expected, or nominal, number of network clock pulses is transmitted from a source node to a destination node in an ATM network. This representation will be referred to hereinafter as the Residual Time Stamp (RTS). By selecting the number of bits, P, so that all 2^P possible different bit patterns uniquely and unambiguously represent the range of possible numbers of network clock cycles within the fixed interval that is defined by N service clock cycles, the destination node can recover the service clock from the common network clock and the received RTS.

At the source node, a free-running P-bit counter counts clock cycles in a clock signal derived from the network clock. The service clock, which is derived from the incoming data signal to be transmitted over the ATM network, is divided by the factor of N to produce a pulse signal having a period (the RTS period) which defines the time interval for measuring the number (modulo 2^P) of derived network clock pulses. At the end of each RTS period, the current count of the free-running P-bit counter is sampled. That sampled value is the RTS, which is transmitted via the adaptation layer. Since the service clock from which the RTS period is defined and the derived network clock are neither synchronized nor integrally related in frequency, the actual number of derived network clock cycles in a RTS period is unlikely to be an integer. Thus, when sampled at the end of each RTS period, the increment in the count of the P-bit counter is a quantized version of the count (modulo 2^P) of pulses in the RTS interval as modified by any accumulated fractional counts from a previous interval.

At the destination node, after the AAL is processed, the successive RTSs are converted into a pulse signal which has periods between pulses defined by the fixed integral numbers of derived network clock pulses that correspond to the conveyed RTS periods. Specifically, a free-running P-bit counter is driven by the derived network clock. A comparator compares this count with a stored received RTS and produces a pulse output upon a match. Since the count of the P-bit counter matches the stored RTS every 2^P derived network clock cycles, comparator output pulses that do not actually represent the end of the RTS period are inhibited by gating circuitry. This gating circuitry includes a second counter that counts the derived network clock cycles occurring since the end of the previous RTS period. When this second counter reaches a count equal to the minimum possible number of derived network clock pulses within an RTS period, the next comparator pulse output produced upon a match between the RTS and the count of the P-bit counter, is gated-through to the output and resets the second counter. The resultant gated through output pulse stream drives a multiply-by-N phase locked loop to recover the service clock.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 are timing diagrams showing the RTS concept of the present invention;

FIG. 2 is a block diagram showing apparatus, in accordance with the present invention, for generating the RTS at the source node of an ATM network;

FIG. 3 is a block diagram showing apparatus, in accordance with the present invention, for reconstructing the service clock at the destination node of an ATM network; and

FIG. 4 are timing diagrams showing the gating function at the apparatus of FIG. 3.

DETAILED DESCRIPTION

The concept of the Residual Time Stamp is described with reference to FIG. 1. In FIG. 1, and in the description hereinafter, the following terminology is used:

f_n—network clock frequency, e.g. 155.52 MHz;

f_{nx}—derived network clock frequency,

$$f_{nx} = \frac{f_n}{x},$$

where x is a rational number;

f_s—service clock frequency;

N—period of RTS in units of the service clock (f_s) cycles;

T_n—the n-th period of the RTS in seconds;

$\pm\epsilon$—tolerance of the source clock frequency in parts per million;

M_n (M_{nom}, M_{max}, M_{min})—number of f_{nx} cycles within the n-th (nominal, maximum, minimum) RTS period, which are, in general, non-integers.

As can be noted in FIG. 1, during the n-th period, T_n, corresponding to N service clock cycles, there are M_n network derived clock cycles. As aforenoted, since the service clock and the network clock are neither synchronized nor integrally related in frequency, this number of derived network clock cycles is not an integer. Since all practical timing recovery techniques transmit only integer values, the fractional part of M_n must be dealt with. Simple truncation or rounding of the fractional part in each RTS time slot is not permissible, as this would lead to a "random walk" type error accumulation. Rather, it is necessary to accumulate the fractional parts at the transmitter and use the accumulated value to modify the transmitted integer quantity. Since it is most convenient to generate RTS by an asynchronous counter, as will be described hereinafter in conjunction with the description of FIG. 2, a "truncation" operation is natural, reflecting the fact that an asynchronous counter's output does not change until the subsequent input pulse arrives. To formalize these notions, S_n is defined as the truncated value of M_n after accounting for the left over fractional part, d_n, from the (n−1)-th interval, viz.,

$$S_n = [M_n + d_n] \tag{1}$$

and

$$d_{n+1} = d_n + M_n - S_n \tag{2}$$

where [a] denotes the largest integer less than or equal to a. Since for accurate clocks, the range of M_n, is very tightly constrained, i.e., $M_{max} - M_{min} = 2y < M_n$, the variation in S_n is also much smaller than its magnitude. It follows from Equation (1) that

$$[M_{min} + d_n] \leqq S_n \leqq [M_{max} + d_n] \tag{3}$$

Since the maximum and minimum of d_n are 1 and 0 respectively, S_n is bounded by,

$$[M_{min}] \leqq S_n \leqq [M_{max}] + 1 \tag{4}$$

This implies, that the most significant portion of S_n carries no information and it is necessary to transmit only its least significant portion. This, therefore, is the essential concept of the RTS. The minimum resolution required to represent the residual part of S_n unambiguously is a function of N, the ratio of the network derived frequency to the service frequency, and the service clock tolerance, $\pm\epsilon$. The maximum deviation, y, between the nominal number of derived network clock pulses in an RTS period, M_{nom}, and the maximum or minimum values of M (M_{max} or M_{min}) is given by,

$$y = N \times \frac{f_{nx}}{f_s} \times \epsilon \tag{5}$$

where M_{nom} equals

$$N \times \frac{f_{nx}}{f_s}.$$

A specific numerical example can be considered for clarity of understanding. As illustrative derived network clock frequency and service clock frequencies could be given by f_{nx}=155.52 MHZ (for x=1), and f_s=78.16 MHz (nominal), respectively. A typical RTS sampling period (N) is 3008, which corresponds to a period of 8 cells and a 47-octet payload per cell (47 bytes/cell×8 bits/byte×8 cells per RTS period). Using these numbers, M_{nom}=5985.2119. If it is further reasonable to assume that the service clock tolerance is 200 parts per million, i.e., $\pm 200 \times 10^{-6}$. From equation (5), therefore, y=1.197, which demonstrates that it is superfluous to transmit the full S_n in each RTS sampling period and transmission of the last few (P) bits of S_n is sufficient. This P-bit sample is the Residual-TS (RTS).

FIG. 2 is a block diagram of the source node of an ATM network showing apparatus for generating and transmitting the RTS. The basic network clock, C, shown at 10, serves as the reference for timing of all nodes of the synchronous network being here considered. This clock, having a frequency f_n, is divided in frequency by a rational factor x by a divider 11 to produce a derived network clock having a frequency f_{nx}. Preferably, x would be an integer value. The dividing factor is chosen so that the P bits available can unambiguously represent the number of derived network clock cycles within an RTS period. In the case where

$$\frac{f_{nx}}{f_s}$$

is less than or equal to two, as in the example above, it can be shown that a 3-bit RTS is sufficient.

The derived network clock, f_{nx}, drives a P-bit counter, which is continuously counting these derived network clock pulses, modulo 2^P. The service clock, f_s, on lead 13, which is derived from the service data signal (not shown) to be transmitted over the ATM network, is divided in frequency by N, the desired RTS period in units of f_s cycles, by divide-by N circuit 14. As shown in FIG. 2, the output of divider 14 is a pulse signal in which T_n is its n-th period. At every T seconds (N source clock cycles) latch 15 samples the current count of counter 12, which is then the P-bit RTS to be transmitted. As aforedescribed, this number represents the residual part of S_n and is all that is necessary to be transmitted to recover the source clock at the destination node of the network.

Each successive RTS is incorporated within the ATM adaptation layer overhead by AAL processor 16. The associated data to be transmitted (not shown) is

also processed by processor 16 to form the payload of the cells, which are then assembled by an ATM assembler 17, which adds an ATM header for transmission over the network 18.

With reference again to the previous example, a four-bit counter (P=4) can be assumed to be used. Since M_{nom}=5985.2119 and 5985.2119 (modulo 16)=1.2119, a typical RTS output sequence when the source is at nominal frequency will be as follows;

. . . 5,6,7,9,10,11,12,13,15,1,2, . . .

Since the counter 16, in effect, quantizes by truncation, the RTS changes only by integer values. The changes in RTS are such that their average is exactly equal to M_{nom} (modulo 2^P). In this example, the changes are either 1 or 2 with the change of 2 occurring either every 4 or 5 RTSs in such a way that the average interval is 1/0.2119=4.7198. In general, successive RTSs are related by

$$RTS_{n+1}=RTS_n+S_n=RTS_n+[d_n+M_n](\text{modulo } 2^P) \quad (6)$$

In order to guarantee that no information is lost due to the modulo arithmetic, i.e., that the transmitted RTS represents S_n unambiguously, it can be seen from equation (4) that the number of bits used for transmission must satisfy:

$$2^P \geq [M_{max}]-[M_{min}]+2 \quad (7)$$

Thus, in the example above, the number of bits allocated to the RTS must be 3 or greater. It can be noted that the number of bits necessary to unambiguously represent the number of derived network clock cycles within the RTS period is substantially less than the number of bits that would be required to represent the absolute number of clock cycles within the same interval. In the example above, for example, a 13-bit number would be required to represent M_{nom}.

If equation (7) is satisfied, knowledge of M_{nom} in the receiver at the destination node along with the received RTSs can be used to reproduce the service clock from the synchronous network clock. FIG. 3 shows one receiver implementation for reproducing the service clock from the received RTSs. At the receiver the common network clock 10 is available as it was at the transmitter. As in the transmitter, a divider 31 divides the network clock frequency, f_n by the same factor of x as divider 11 in the source node, to produce the same derived network clock signal having a frequency f_{nx} as was used by the transmitter at the source node of FIG. 2.

In a structure paralleling the transmitter in FIG. 2, a disassembler 32 processes the ATM headers received from the network 18 and passes the payload to an AAL processor 33. In addition to extracting the transmitted data (not shown), processor 33 extracts the periodic transmitted RTSs, which are sequentially stored in a FIFO 34, which is used to absorb the network cell jitter. The earliest received RTS in FIFO 34 is compared by P-bit comparator 35 with the count of a free running P-bit counter 36, driven by the derived network clock, f_{nx}. Whenever the output of counter 36 matches the current RTS, comparator 35 generates a pulse. Since counter 36 is a modulo 2^P counter, the RTS in FIFO 34 matches the count of counter 36 every 2^P derived network clock pulses, f_{nx}. The output of comparator 35 thus consists of a train of pulses that are separated, except for the first pulse, by 2^P cycles of the derived network clock. In order to select the output pulse of comparator 35 that corresponds to the end of the fixed period of the transmitted service clocks, which is the period per RTS to be recovered, gating circuitry 37 is employed. Gating circuitry 37, which includes a counter 38, a gating signal generator 39, and an AND gate 40, gates only that pulse output of comparator 35 produced after counting, from the last gated output pulse, a minimum number, M_l, of derived network clock cycles. This minimum number, M_l, is given by:

$$M_l=[M_{nom}]-2^{(P-1)} \quad (8)$$

This ensures that $[M_{max}]-2^P<M_l<[M_{min}]$, and thus the gating pulse is guaranteed to select the correct RTS.

The gating function is best explained in conjunction with the timing diagrams of FIG. 4. Initially, it can be assumed that gating signal generator 39 is set to keep AND gate 40 open. Comparator 35 compares the first RTS in FIFO 34 with the free-running count of counter 36. When the count of counter 36 matches this first RTS, shown in FIG. 4 as "2", comparator 35 produces a pulse which is gated through AND gate 40. This gated output pulse resets gating signal generator 39 thereupon turning off AND gate 40, resets the counter of counter 38 to zero, and reads the next stored RTS, "5", in FIFO 34. When counter 36 reaches the count of "5", comparator 35 produces another output pulse. AND gate 40, however, is OFF and remains off until counter 38 counts M_l derived network clock cycles. Therefore, as noted in FIG. 4, all the subsequent matches of the RTS, "5" and the count of counter 36, which occur every 2^P derived network clock cycles, are blocked by AND gate 40. These subsequent pulses are blocked until counter 38 reaches a count of that minimum number of clock cycles that can comprise the fixed interval to be recovered from the RTS. After counting M_l derived network clock cycles, counter 38 generates a pulse which signals gating signal generator 39 to open AND gate 40. The next pulse produced by comparator 35 upon the match between the RTS in FIFO 34 and the count of counter 36 is gated through AND gate 40. This pulse, as before, resets counter 38, resets gating signal generator 39, and reads-in the next stored RTS to the output of FIFO 34. The resultant time difference between output pulses of AND gate 40 is the desired fixed time interval, S_n, to be recovered from the transmitted RTSs. As previously defined in equation (1), S_n is the truncated value in the nth interval, after accounting for a left over portion from the (n−1)-th interval, of the actual number of derived network clock cycles within the fixed interval defined by N source clock cycles. As can be noted, S_n modulo (2^P) is equal to the difference of the RTSs associated with the pulses matched by comparator 35 right before and right after the reset. Thus in FIG. 4, for the n-th period, this is the difference between "5" and "2", or "3", and for the (n+1)-st period, this is the difference between "9" and "5" or "4". The resultant pulse train at the output of gating circuitry 37 can be seen to duplicate the signal at the source node of the network, which is defined by N service clock cycles, as modified by the quantization effect of the RTSs. This pulse stream is input to a multiply-by N phase-locked loop 41 which multiplies the frequency by the factor of N and smooths out the variation of the reproduced periods. The resultant output

clock signal, f_r, is the reproduced service timing signal, which can be employed by the circuitry at the destination node.

The above-described embodiment is illustrative of the principles of the present invention. Other embodiments could be devised by those skilled in the art without departing from the spirit and scope of the present invention.

What is claimed is:

1. A method of recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising the steps of:

(a) at the source node, dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

(b) at the source node, counting the network clock cycles modulo 2^P, where 2^P is less than the number of network clock cycles within an RTS period and P is chosen so that the 2^P counts uniquely and unambiguously represent the range of possible network clock cycles within an RTS period;

(c) transmitting from the source node to the destination node an RTS at the end of each RTS period that is equal to the modulo 2^P count of network clock cycles at that time;

(d) determining from the RTSs received at the destination node, the number of network clock cycles in each RTS period;

(e) generating a pulse signal from the network clock at the destination node in which the period between each pulse in the pulse signal equals the determined number of network clock cycles in the corresponding RTS period; and

(f) multiplying the frequency of the pulse signal generated in step (e) by the same factor of an integer N used in step (a) to recover the timing clock of the service input.

2. The method of claim 1 wherein the network clock frequency is less than or equal to twice the service clock frequency.

3. A method of recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising the steps of:

(a) at the source node, dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

(b) at the source node, dividing the network clock by a rational factor to form a derived network clock;

(c) at the source node, counting the derived network clock cycles modulo 2^P, where 2^P is less than the number of derived network clock cycles within an RTS period and P is chosen so that the 2^P counts uniquely and unambiguously represent the range of possible derived network clock cycles within an RTS period;

(d) transmitting from the source node to the destination node an RTS at the end of each RTS period that is equal to the modulo 2^P count of derived network clock cycles at that time;

(e) at the destination node, dividing the network clock by the same rational factor used at the source node to form a derived network clock equal to the derived network clock at the source node;

(f) determining from the RTSs received at the destination node, the number of derived network clock cycles in each RTS period;

(g) generating a pulse signal from the derived network clock at the destination node in which the period between each pulse in the pulse signal equals the determined number of derived network clock cycles in the corresponding RTS period; and

(h) multiplying the frequency of the pulse signal generated in step (g) by the same factor of an integer N used in step (a) to recover the timing clock of the service input.

4. The method of claim 3 wherein the derived network clock frequency is less than or equal to twice the service clock frequency.

5. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising at the source node:

dividing means for dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

counting means connected to the network clock for counting network clock cycles modulo 2^P, where 2^P is less than the number of network clock cycles within an RTS period and P is chosen so that the 2^P counts uniquely and unambiguously represent the range of possible network clock cycles within an RTS period; and

transmitting means, responsive to the RTS periods formed by said dividing means and the count of said counting means, for transmitting over the telecommunications network an RTS at the end of each RTS period that is equal to the modulo 2^P count of network clock cycles at that time;

and comprising at the destination node:

receiving means for receiving the RTSs transmitted over the telecommunications network by said transmitting means;

converting means responsive to the received RTSs and the network clock for converting the received RTSs into a pulse signal in which the periods between pulses are determined from the numbers of network clock cycles associated with the counts of network clock cycles within said RTS periods; and

means for multiplying the frequency of the pulse signal generated by said converting means by the same factor of an integer N used in said dividing means for recovering the timing clock of the service input.

6. Apparatus in accordance with claim 5 wherein the network clock frequency is less than or equal to twice the service clock frequency.

7. Apparatus in accordance with claim 5 wherein said converting means comprises:

means for sequentially storing the received RTSs;

means for counting network clock cycles modulo 2^P;

comparing means for comparing the modulo 2^P count of network clock cycles with a stored RTS and for generating a pulse each time the count of network clock cycles matches the RTS; and

gating means for gating to said multiplying means, for each sequentially received and stored RTS, the pulse produced by said comparing means that oc-

curs after the counting means counts, starting-in-time from the previous gated pulse, a number of network clock cycles that is greater than a predetermined minimum absolute number of network clock cycles that can occur within any RTS period.

8. Apparatus for recovering, at a destination node of a packet-based telecommunications network, the timing clock of a service input at a source node of said packet-based telecommunications network, the destination node and the source node having a common network clock, comprising at the source node:

first dividing means for dividing the timing clock of the service input by a factor of an integer N to form residual time stamp (RTS) periods;

second dividing means for dividing the network clock by a rational factor to form a derived network clock;

counting means connected to the network clock for counting derived network clock cycles modulo 2^P, where 2^P is less than the number of derived network clock cycles within an RTS period and P is chosen so that the 2^P counts uniquely and unambiguously represent the range of possible derived network clock cycles within an RTS period; and

transmitting means, responsive to the RTS periods formed by said first dividing means and the count of said counting means, for transmitting over the telecommunications network an RTS at the end of each RTS period that is equal to the modulo 2^P count of derived network clock cycles at that time;

and comprising at the destination node:

receiving means for receiving the RTSs transmitted over the telecommunications network by said transmitting means;

means for dividing the network clock by the same rational factor used at the source node to form a derived network clock;

converting means responsive to the received RTSs and the derived network clock for converting the received RTSs into a pulse signal in which the periods between pulses are determined from the numbers of derived network clock cycles associated with the counts of derived network clock cycles within said RTS periods; and

means for multiplying the frequency of the pulse signal generated by said converting means by the same factor of an integer N used in said first dividing means for recovering the timing clock of the service input.

9. Apparatus in accordance with claim 8 wherein the derived network clock frequency is less than or equal to twice service clock frequency.

10. Apparatus in accordance with claim 8 wherein said converting means comprises:

means for sequentially storing the received RTSs;

means for counting derived network clock cycles modulo 2^P;

comparing means for comparing the modulo 2^P count of derived network clock cycles with a stored RTS and for generating a pulse each time the count of derived network clock cycles matches the RTS; and

gating means for gating to said multiplying means, for each sequentially received and stored RTS, the pulse produced by said comparing means that occurs after the counting means counts, starting-in-time from the previous gated pulse, a number of derived network clock cycles that is greater than a predetermined minimum absolute number of derived network clock cycles that can occur within any RTS period.

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EXHIBIT C

REDACTED